

Reliability Report

General Information	
Product Line	<i>U371</i>
Product Description	<i>HIGH VOLTAGE GATE DRIVER</i>
Product division	<i>I&PC</i>
Package	<i>S08</i>
Silicon process technology	<i>BCD OFF LINE</i>

Locations	
Wafer fab location	<i>AMK</i>
Assembly plant location	<i>ST SHENZHEN CHINA</i>
Reliability assessment	<i>Pass</i>

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	01-dec-2016	10	G. D'Angelo	Original document
2.0	24-Feb-17	11	G. D'Angelo	Updated with Package Oriented test on U371 device

Issued by

Gianfranco D'Angelo

Approved by

Federico Fieschi

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
0061692	: Reliability tests and criteria for qualifications

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of U371 device diffused in AMK and assembled in SO8 in ST SHENZHEN CHINA in the overall plan of LeadFrame change in Shenzhen.

Considering that U371 device is assembled in the same plant with the same package and the same leadframe of U324, the positive results obtained from U324 can be extended to U371 device.

According to Reliability Qualification Plan, below is the list of the overall trials performed on samples with new LeadFrame:

Die Oriented Tests (on U324 device)

- High Temperature Operating Life
- Early Life Failure Rate

Package Oriented Tests (on U324 device)

- Preconditioning
- Temperature Cycling
- Autoclave
- High Temperature Storage Life
- Temperature Humidity Bias
-

Package Oriented Tests (on U371 device)

- Preconditioning
- Temperature Cycling

Electrical Characterization (on U371 device)

- ESD resistance test
- LATCH-UP resistance test

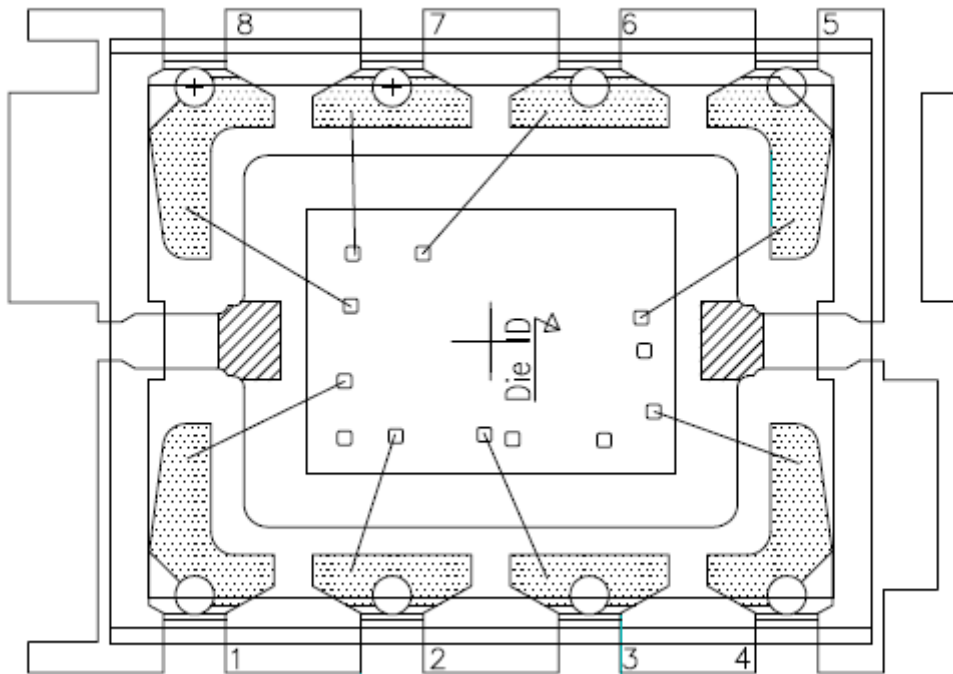
2.2 Conclusion

Taking in account the results of the trials performed **the U371 diffused in AMK and assembled in SO8 in ST SHENZHEN CHINA can be qualified from reliability viewpoint.**

3 DEVICE CHARACTERISTICS

3.1 Device description

3.1.1 Bonding Diagram



3.2 Traceability

Wafer fab information

Wafer fab manufacturing location	<i>AMK</i>
Wafer diameter	<i>6 inches</i>
Wafer thickness	<i>375um</i>
Silicon process technology	<i>BCD OFF LINE</i>
Die finishing back side	<i>Cr/Ni</i>
Die size	<i>2370x1700 um</i>
Passivation	<i>SiN</i>
Metal levels	<i>1</i>

Assembly Information

Assembly plant location	<i>ST SHENZHEN CHINA</i>
Package description	<i>SO8</i>
Molding compound	<i>G700</i>
Wires bonding materials/diameters	<i>Cu/1 mils</i>
Die attach material	<i>8601</i>
Lead solder material	<i>NiPdAu</i>

4 TESTS RESULTS SUMMARY

4.1 LOTS information

Lot ID #	Silicon Rev.
1	AEA (U324 device)
2	AEA (U324 device)
3	AEA (U324 device)
4	BC6 (U371 device)

4.2 Test plan and results summary

Die Oriented Tests (performed on U324 assembled in Shenzhen in SO8 package)							
Test	Method	Conditions	Failure/SS			Duration	Note
			Lot 1	Lot 2	Lot 3		
HTOL	High Temperature Operating Life						
	PC before	Tj=150°C, VCC=17V	0/77	0/77	0/77	1000h	
ELFR	Early Life Failure Rate						
		Tj=150°C, VCC=17V	0/800	0/800	0/800	24h	

Package Oriented Tests (performed on U324 assembled in Shenzhen in SO8 package)							
Test	Method	Conditions	Failure/SS			Duration	Note
			Lot 1	Lot 2	Lot 3		
PC	Pre-Conditioning: Moisture sensitivity level 3						
		192h 30°C/60% - 3 reflow PBT 260°C	0/231	0/231	0/231		
THB	Temperature Humidity Bias						
	PC before	Ta=85°C/85%RH VCC=17V	0/77	0/77	0/77	1000h	
AC	Autoclave						
	PC before	121°C 2atm	0/77	0/77	0/77	96h	
TC	Temperature Cycling						
	PC before	Temp. range: -50/+150°C	0/77	0/77	0/77	2000cy	
HTSL	High Temperature Storage						
	No bias	Tamb=150°C	0/45	0/45	--	1000h	

Package Oriented Tests (performed on U371)							
Test	Method	Conditions	Failure/SS			Duration	Note
			Lot 4				
PC3	Pre-Conditioning: Moisture sensitivity level 3						
		192h 30°C/60% - 3 reflow PBT 260°C	0/77				
PC1	Pre-Conditioning: Moisture sensitivity level 1						
		168h 85°C/85% - 3 reflow PBT 260°C	0/77				
TC	Temperature Cycling						
	PC3 before	Temp. range: -50/+150°C	0/77			1000cy	
TC	Temperature Cycling						
	PC1 before	Temp. range: -50/+150°C	0/77			1000cy	

Electrical Characterization Tests (performed on U371)						
Test	Method	Conditions	Sample/Lots	Number of lots	Duration	Results
ESD	Electro Static Discharge (performed on SO8)					
	Human Body Model	+/- 2kV	3	1		PASSED
	Machine Model	+/- 200V	3	1		PASSED
	Charge Device Model	+/- 500V (+/-750V on corner pins)	3	1		PASSED
LU	Latch-Up (performed on PDIP)					
	Over-voltage and Current Injection	Tamb=25°C Jedec78	6	1		PASSED

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Die oriented tests

5.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

5.1.2 Early Life Failure Rate

This test is to evaluate the defects inducing failure in early life.

The device is stressed in biased conditions at the max junction temperature.

The read-outs flow chart is the following:

- Initial testing @ Ta=25°C
- Final Testing (24 hr.) @ Ta=25°C

5.2 Package oriented tests

5.2.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.

The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

5.2.2 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.

The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

5.2.3 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.

Test flow chart is the following:

- Initial testing @ $T_a=25^{\circ}\text{C}$.
- Readout @ 500 cycles.
- Final Testing @ 1000 cycles @ $T_a=25^{\circ}\text{C}$.

TEST CONDITIONS:

- $T_a= -50^{\circ}\text{C}$ to $+150^{\circ}\text{C}$ (air)
- 15 min. at temperature extremes
- 1 min. transfer time

5.2.4 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.

Test flow chart is the following:

- Initial testing @ $T_a=25^{\circ}\text{C}$.
- Final Testing (168hrs or 240hrs) @ $T_a=25^{\circ}\text{C}$.

TEST CONDITIONS:

- $P=2.08$ atm
- $T_a=121^{\circ}\text{C}$
- test time= 168hrs or 240hrs

5.2.5 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die-package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.

The device is stressed in static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions => $T_a=85^{\circ}\text{C}$ / RH=85%.

Input pins to Low / High Voltage (alternate) to maximize voltage contrast.

Test Duration 1000 h.

The flow chart is the following:

- Initial testing @ $T_a=25^{\circ}\text{C}$
- Check @ 168 and 500hrs
- Final Testing (1000 hr.) @ $T_a=25^{\circ}\text{C}$

5.3 Electrical Characterization Tests

5.3.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up. The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
<i>IN low</i>	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less
<i>IN high</i>	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less

5.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.

The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** ANSI/ESDA/JEDEC STANDARD JES001
CDF-AEC-Q100-002
- **Machine Model** JEDEC STANDARD EIA/JESD-A115
CDF-AEC-Q100-003
- **Charge Device Model** ANSI/ESD STM 5.3.1 ESDA – JEDEC JESD22-C101
CDF-AEC-Q100-011